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Docket No.: WMP-IFT-964

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MAIL STOP: APPEAL BRIEF-PATENTS

By: Wenghong Chen Date: February 28, 2006

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Before the Board of Patent Appeals and Interferences

Applic. No.	:	10/657,898 Confirmation No.: 5647
Inventor	:	Thomas Steinecke, et al.
Filed	:	September 9, 2003
Title	:	Electronic Device with a Voltage Supply Structure, Semiconductor Wafer with Electronic Devices, and Associated Production Methods
TC/A.U.	:	2814
Examiner	:	Phat X. Cao
Customer No.	:	**24131**

Hon. Commissioner for Patents
Alexandria, VA 22313-1450

APPEAL BRIEF

S i r :

This is an appeal from the final rejection in the Office action dated July 25, 2005, finally rejecting claims 1-3, 6-13, and 16-17.

Appellants submit this *Appeal Brief*, including payment in the amount of $500.00 to cover the fee for filing the *Appeal Brief*.

Real Party in Interest:

This application is assigned to Infineon Technologies AG of München, Germany. The assignment will be submitted for recordation upon the termination of this appeal.

Related Appeals and Interferences:

No related appeals or interference proceedings are currently pending which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

Status of Claims:

Claims 1-3, 6-13, and 16-17 are rejected and are under appeal. Claims 4, 5, and 14-15 are objected to. Claims 18 and 19 are withdrawn from consideration.

Status of Amendments:

No claims were amended after the final Office action. A *Notice of Appeal* was filed on December 30, 2005.

Summary of the Claimed Subject Matter:

The invention of the instant application concerns an electronic device including a semiconductor chip (7) having an active top side (8) with a plurality of contact areas (18). See, for example, Fig. 2 and page 22, lines 3-4 of the specification. The semiconductor chip has a plurality of

metallization layers (1-6) and a plurality of insulation layers (11-15) configured alternately one above another on the active top side. See, for example, Fig. 2 and page 21, lines 23-24 and page 23, lines 6-7 of the specification. The plurality of metallization layers (1-6) include topmost metallization layers (5-6) having a plurality of voltage supply structures (9) and lower metallization layers (1-4) disposed underneath the topmost metallization layers and having a plurality of signal line structures (10). See, for example, Figs. 2-3 and page 22, lines 8-10 and page 24, lines 14-16 of the specification. The plurality of insulation layers (11-15) are formed with a plurality of passage contacts (17) connecting the plurality of voltage supply structures (9) and/or the plurality of signal line structures (10) to the plurality of contact areas (18) of the active top side (8). See, for example, Figs. 2-3 and page 23, line 7 of the specification. The topmost metallization layers (5-6) have ones of the plurality of passage contacts (17) connected to the plurality of contact areas (18). See, for example, Figs. 2-3 and page 24, lines 22-23 of the specification. The topmost metallization layers (5-6) have at least a first one of the plurality of voltage supply structures (9) for a low supply potential (-) and a second one of the plurality of voltage supply structures (9) for a high supply potential (+). See, for example, Fig. 4 and page 25, lines 7-9 and lines 16-

17 of the specification. The first one of the plurality of voltage supply structures is insulated from the second one of the plurality of voltage supply structures. See, for example, Fig. 5 and page 26, lines 16-19 of the specification. The first one of the plurality of voltage supply structures of the topmost metallization layers has a grid of supply interconnects (20) configured parallel to one another. The second one of the plurality of voltage supply structures (9) of the topmost metallization layers has a grid of supply interconnects (20) configured parallel to one another. The grid of supply interconnects of the first one of the plurality of voltage supply structures is rotated relative to the grid of supply interconnects of the second one of the plurality of voltage supply structures. See, for example, Figs. 4-7 and page 25, lines 16-19 of the specification.

The invention of the instant application also concerns a semiconductor wafer including an active top side having a plurality of contact areas and a plurality of semiconductor chip positions configured in rows and columns on the active top side. See page 1, lines 10-13 of the specification. Each one of the plurality of semiconductor chip positions has a plurality of patterned metallization layers and a plurality of insulation layers configured alternately one above another. The plurality of insulation layers have a plurality of passage

contacts. The plurality of metallization layers include topmost metallization layers having a plurality of area-covering voltage supply structures and lower metallization layers disposed underneath the topmost metallization layers and having a plurality of signal line structures. The plurality of passage contacts are configured in said insulation layers connecting the plurality of voltage supply structures and/or the plurality of signal line structures of the metallization layers to the plurality of contact areas on the active top side. In each one of the plurality of semiconductor chip positions, the topmost metallization layers have at least a first one of the plurality of voltage supply structures for a low supply potential and a second one of the plurality of voltage supply structures for a high supply potential. The first one of the plurality of voltage supply structures is insulated from the second one of the plurality of voltage supply structures. Each one of the plurality of semiconductor chip positions includes a contact wire layer and a plurality of module regions configured below the topmost metallization layers. In each one of the plurality of semiconductor chip positions, the topmost metallization layers have a plurality of passage contacts for electrically connecting the first one of the plurality of voltage supply structures and the second one of said plurality of voltage supply structures to the plurality of module regions via the

contact wire layer. In each one of the plurality of semiconductor chip positions, the first one of the plurality of voltage supply structures of the topmost metallization layers has a grid of supply interconnects configured parallel to one another. In each one of the plurality of semiconductor chip positions, the second one of the plurality of voltage supply structures of the topmost metallization layers has a grid of supply interconnects configured parallel to one another. In each one of the plurality of semiconductor chip positions, the grid of supply interconnects of the first one of the plurality of voltage supply structures is rotated relative to the grid of supply interconnects of the second one of the plurality of voltage supply structures.

References Cited:

5,949,098	Mori	September 7, 1999
6,696,712	Yonesaka	February 24, 2004
6,825,553	Chua, et al.	November 30, 2004

Grounds of Rejection to be Reviewed on Appeal

1. Whether or not claims 1-3 and 6-10 are obvious over Mori in view of Yonesaka under 35 U.S.C. §103(a).

2. Whether or not claims 11-13 and 16-17 are obvious over Mori in view of Yonesaka and Chua et al. under 35 U.S.C. §103(a).

Argument:

Claims 1-3 and 6-10 are not obvious over Mori in view of Yonesaka under 35 U.S.C. §103(a).

In item 2 on pages 2-5 of the above-mentioned Office action, claims 1-3 and 6-10 have been rejected as being unpatentable over Mori in view of Yonesaka under 35 U.S.C. § 103(a).

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 1 calls for, inter alia:

> said grid of supply interconnects of said first one of said plurality of voltage supply structures being rotated relative to said grid of supply interconnects of said second one of said plurality of voltage supply structures.

According to the invention of the instant application, the grid (21) of the supply interconnects (20) of the first one of the plurality of voltage supply structures (9) in one of the topmost metallization layers (6) is rotated relative to (or more specifically oriented orthogonally to) the grid (19) of the supply interconnects (20) of the second one of plurality of voltage supply structures (9) in the other one of the topmost metallization layers (5). This can be clearly been, for example, in Fig. 4 and is clearly described on page 24, lines 14-18 and page 25, lines 16-19 of the specification.

The Examiner has stated that Fig. 3 of Mori clearly discloses the grid of supply interconnects 332 of the first one of the plurality of voltage supply structures being rotated parallel relative to the grid of supply interconnects 331 of the second one of the plurality of voltage supply structures (see page 8, lines 6-9 of the final Office action). The Examiner has further stated that since the claims should be given their broadest reasonable interpretation, the phrase "being rotated" can be interpreted as "being rotated" in any direction including "parallel" (see the last paragraph on page 8 of the final Office action).

However, it is noted the words of a claim must be given their "plain meaning," namely the ordinary and customary meaning that the term would have to a person of ordinary skill in the art at the time of the invention. See MPEP 2111.01. In this case, a person of ordinary skill in the art at the time of the invention would understand from the term "being rotated relative to" that the two grids of supply interconnects are offset in certain degree in their orientation. In the embodiments shown, for example, in Fig. 4 of the instant application, the two grids are oriented orthogonally. "Parallel" orientation cannot be considered to be covered under the term "being rotated relative to" even in its

broadest interpretation. Rather, "parallel" means that there is not any rotation.

Clearly, Mori does not show "said grid of supply interconnects of said first one of said plurality of voltage supply structures being rotated relative to said grid of supply interconnects of said second one of said plurality of voltage supply structures," as recited in claim 1 of the instant application. Yonesaka does not make up for the deficiencies of Mori.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 1. Claim 1 is, therefore, believed to be patentable over the art and since dependent claims 2-3 and 6-10 are dependent on claim 1, they are believed to be patentable as well.

Claims 11-13 and 16-17 are not obvious over Mori in view of Yonesaka and Chua et al. under 35 U.S.C. §103(a)

In item 3 on pages 5-7 of the above-mentioned Office action, claims 11-13 and 16-17 have been rejected as being unpatentable over Mori in view of Yonesaka and Chua et al. under 35 U.S.C. § 103(a).

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 11 calls for, inter alia:

> said grid of supply interconnects of said first one of said plurality of voltage supply structures being rotated relative to said grid of supply interconnects of said second one of said plurality of voltage supply structures.

The above discussion with regard to claim 1 of the instant application also applies to claim 11.

Clearly, Mori does not show "said grid of supply interconnects of said first one of said plurality of voltage supply structures being rotated relative to said grid of supply interconnects of said second one of said plurality of voltage supply structures," as recited in claim 11 of the instant application. The other cited references do not make up for the deficiencies of Mori.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 11. Claim 11 is, therefore, believed to be patentable over the art and since dependent claims 12-13 and 16-17 are dependent on claim 11, they are believed to be patentable as well.

In view of the foregoing, the honorable Board is therefore respectfully urged to reverse the final rejection of the Primary Examiner.

Respectfully submitted,

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Claims Appendix:

1. An electronic device, comprising:

a semiconductor chip having an active top side with a plurality of contact areas;

said semiconductor chip having a plurality of metallization layers and a plurality of insulation layers configured alternately one above another on said active top side;

said plurality of metallization layers including topmost metallization layers having a plurality of voltage supply structures and lower metallization layers disposed underneath said topmost metallization layers and having a plurality of signal line structures;

said plurality of insulation layers formed with a plurality of passage contacts connecting said plurality of voltage supply structures and/or said plurality of signal line structures to said plurality of contact areas of said active top side;

said topmost metallization layers having ones of said plurality of passage contacts connected to said plurality of contact areas;

said topmost metallization layers having at least a first one of said plurality of voltage supply structures for a low supply potential and a second one of said plurality of voltage supply structures for a high supply potential;

said first one of said plurality of voltage supply structures being insulated from said second one of said plurality of voltage supply structures;

said first one of said plurality of voltage supply structures of said topmost metallization layers having a grid of supply interconnects configured parallel to one another;

said second one of said plurality of voltage supply structures of said topmost metallization layers having a grid of supply interconnects configured parallel to one another; and

said grid of supply interconnects of said first one of said plurality of voltage supply structures being rotated relative

to said grid of supply interconnects of said second one of said plurality of voltage supply structures.

2. The electronic device according to claim 1, wherein:

said semiconductor chip includes an integrated circuit subdivided into a plurality of functional module regions; and

each one of said plurality of module regions has a plurality of passage contacts connecting ones of said plurality of contact areas to said first one of said plurality of voltage supply structures and to said second one of said plurality of voltage supply structures.

3. The electronic device according to claim 1, wherein:

said semiconductor chip has a silicon chip made of monocrystalline material and has an integrated circuit near said active top side;

said integrated circuit has said plurality of contact areas and a plurality of interconnects configured above said plurality of contact areas;

said plurality of interconnects of said integrated circuit and said plurality of contact areas have electrical connections therebetween;

said electrical connections are effected via said plurality of passage contacts of said plurality of insulation layers; and

said electrical connections are wired automatically using place-route programs.

6. The electronic device according to claim 1, wherein:

said supply interconnects of said grid of said first one of said plurality of voltage supply structures all have a first electrical supply potential; and

said supply interconnects of said grid of said second one of said plurality of voltage supply structures all have a second electrical supply potential that is different from said first electrical supply potential.

7. The electronic device according to claim 1, wherein ones of said plurality of insulation layers located between said topmost metallization layers have a thickness dimensioned to

provide an electrical capacitance that is as high as possible with sufficient dielectric strength at areas of said topmost metallization layers that are configured one above another.

8. The electronic device according to claim 1, wherein said plurality of metallization layers include polycrystalline silicon, copper, aluminum, nickel, an alloy of copper, an alloy of aluminum, or an alloy of nickel.

9. The electronic device according to claim 1, wherein said plurality of insulation layers include silicon dioxide, silicon nitride, or polymeric plastics.

10. The electronic device according to claim 1, wherein:

said plurality of signal line structures have interconnects with a thickness and a width;

said supply interconnects of said grid of said first one of said plurality of voltage supply structures have a thickness and a width that are greater than said thickness and said width of said interconnects of said plurality of signal line structures; and

said supply interconnects of said grid of said second one of said plurality of voltage supply structures have a thickness and a width that are greater than said thickness and said width of said interconnects of said plurality of signal line structures.

11. A semiconductor wafer, comprising:

an active top side having a plurality of contact areas;

a plurality of semiconductor chip positions configured in rows and columns on said active top side;

each one of said plurality of semiconductor chip positions having a plurality of patterned metallization layers and a plurality of insulation layers configured alternately one above another, said plurality of insulation layers having a plurality of passage contacts, said plurality of metallization layers including topmost metallization layers having a plurality of area-covering voltage supply structures and lower metallization layers disposed underneath said topmost metallization layers and having a plurality of signal line structures, said plurality of passage contacts configured in said insulation layers connecting said plurality of voltage supply structures and/or said plurality

of signal line structures of said metallization layers to said plurality of contact areas on said active top side;

in each one of said plurality of semiconductor chip positions, said topmost metallization layers having at least a first one of said plurality of voltage supply structures for a low supply potential and a second one of said plurality of voltage supply structures for a high supply potential, said first one of said plurality of voltage supply structures being insulated from said second one of said plurality of voltage supply structures;

each one of said plurality of semiconductor chip positions including a contact wire layer and a plurality of module regions configured below said topmost metallization layers;

in each one of said plurality of semiconductor chip positions, said topmost metallization layers having a plurality of passage contacts for electrically connecting said first one of said plurality of voltage supply structures and said second one of said plurality of voltage supply structures to said plurality of module regions via said contact wire layer;

in each one of said plurality of semiconductor chip positions, said first one of said plurality of voltage supply structures of said topmost metallization layers having a grid of supply interconnects configured parallel to one another;

in each one of said plurality of semiconductor chip positions, said second one of said plurality of voltage supply structures of said topmost metallization layers having a grid of supply interconnects configured parallel to one another; and

in each one of said plurality of semiconductor chip positions, said grid of supply interconnects of said first one of said plurality of voltage supply structures being rotated relative to said grid of supply interconnects of said second one of said plurality of voltage supply structures.

12. The wafer according to claim 11, wherein:

each one of said plurality of semiconductor chip positions includes an integrated circuit subdivided into a plurality of functional module regions; and

each one of said plurality of module regions has a plurality of passage contacts connecting ones of said plurality of

contact areas to said first one of said plurality of voltage supply structures and to said second one of said plurality of voltage supply structures in said one of said plurality of module regions.

13. The wafer according to claim 11, further comprising:

a silicon chip made of monocrystalline material; and

an integrated circuit near said active top side;

said integrated circuit having ones of said plurality of contact areas and a plurality of interconnects configured above said ones of said plurality of contact areas of said integrated circuit;

said plurality of interconnects of said integrated circuit and said ones of said plurality of contact areas of said integrated circuit having electrical connections therebetween;

said electrical connections effected via said plurality of passage contacts of said plurality of insulation layers; and

said electrical connections being wired automatically using place-route programs.

16. The wafer according to claim 11, wherein:

said supply interconnects of said grid of said first one of said plurality of voltage supply structures all have a first electrical supply potential; and

said supply interconnects of said grid of said second one of said plurality of voltage supply structures all have a second electrical supply potential that is different from said first electrical supply potential.

17. The wafer according to claim 11, wherein ones of said plurality of insulation layers located between said topmost metallization layers have a thickness dimensioned to provide an electrical capacitance that is as high as possible with sufficient dielectric strength at areas of said topmost metallization layers that are configured one above another.

Evidence Appendix:

No evidence pursuant to && 1.130, 1.131, or 1.132 or any other evidence has been entered by the Examiner and relied upon by appellant in the appeal.

Related Proceedings Appendix:

Since there are no prior or pending appeals, interferences or judicial proceedings which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in this appeal, no copies of decision rendered by a court or the Board are available.